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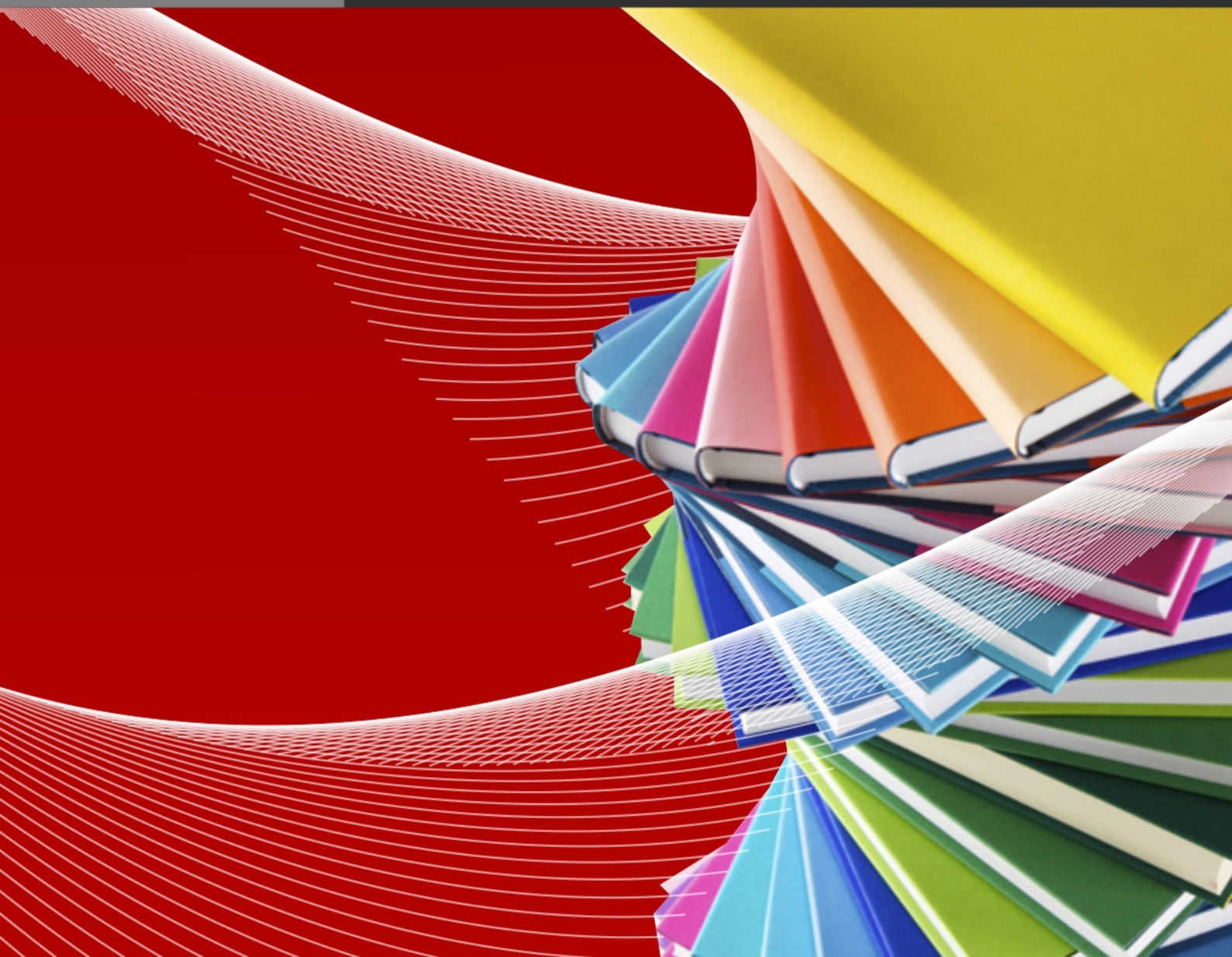

Fully Integrated High Voltage MEMS Drivers in CMOS

by

LEI KA CHON

Final Year Project Report submitted in partial fulfillment
of the requirements for the Degree of

Bachelor of Science in Electrical and Computer Engineering

2016/2017

Faculty of Science and Technology
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APPROVAL FOR SUBMISSION

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Mainly focus on the design, analysis and simulation of the charge pump.

ABSTRACT

We present the design of a fully-integrated high-voltage MEMS driver with an on-chip charge pump in 65nm CMOS technology. Bulk CMOS is mainly limited by the breakdown voltage transistors as well as that of the well/substrate diode. To operate in a high voltage environment (in the order of 10V), we applied the NWell/Psub and DNWell/Psub diodes which satisfy the described conditions. The proposed charge pump is composed of a 4-stage charge pump, which demonstrates a four-fold voltage increment at the output. Also, the charge pump design features MOSFET to replace the diode to eliminate the efficiency loss due to the diode voltage drop. The high-voltage driver is designed to reduce the energy loss and handle the 10V charge pump output while preventing the CMOS transistor breakdown, capable of producing a 250-kHz square wave at 10 V.

A chip prototype is fabricated in standard 65nm CMOS technology, with the 4-stage charge pump and high-voltage driver occupying 0.1 and 0.12 mm^2, respectively. This work achieves a peak charge pumps efficiency of 68.6%, with an input parasitic sensor capacitance and the charge pump loading capacitance of 5pF and 67pF, respectively. By eliminating the discharging of the charge pump during the driver output transitions, the proposed driver achieves a driving efficiency of 40.86%, which is almost 9X improvement when compared with the state of the art.

Keywords - Charge Pump; high voltage driver; high efficiency.

TABLE OF CONTENTS

CHAPTER 4 EXPERIMENTAL RESULTS

CHAPTER 5 SUMMARY OF THIS WORK

LIST OF TABLES/FIGURES

CHAPTER 1 INTRODUCTION

1.1 Background

Nowadays, each smartphone is equipped with about four to eight MEMS devices to improve the user experience by sensing the ambient environment, resulting in the continuous growth in the MEMS shipments [1], as shown in Figure 1. For portable electronic devices such as the cellular phone and GPS, a low phase noise environment is required. The MEMS resonators are passive devices that are electrostatically driven by the sustaining circuit. One solution is to bias the MEMS resonator with a high-level DC voltage to reduce its motional impedance and increase the output current, thereby increasing the energy of the signal. To achieve high energy efficiency, advanced CMOS processes work in low-voltage supplies, which is a major issue in high voltage MEMS driver design. To solve this problem, a charge pump is needed to provide a high voltage to bias the MEMS resonator [2].

The motivation of this project is to resolve the high operating voltage requirement for MEMS using advanced CMOS technology with low supply voltage for system cost reduction. For the state of the art [2], even though they can achieve a peak charge pump efficiency of 77%, the respective driver efficiency is only 4.35% by directly driving the MEMS device using the charge pump output. This induces wasteful charging and discharging process of the loading capacitor which inevitably sacrifices the system efficiency. This can also be resulting in a poor rise and fall time of the driver as a result of the increase loading capacitance. In this work, two switches are implemented to isolate the loading capacitor of the charge pump and the parasitic capacitor of the MEMS, which means that after the charge pump has boosted the on-

chip low voltage to a high voltage, it will pass through the high-voltage driver to bias the MEMS resonator. The detailed implementation will be discussed in Chapter 3.

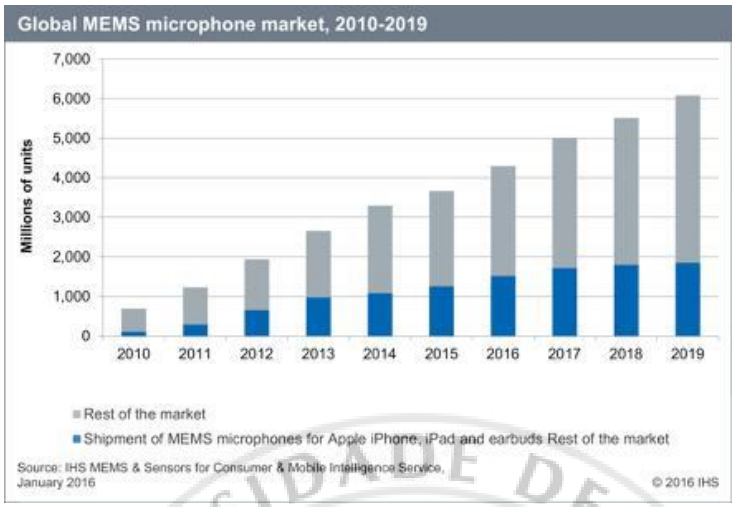

Figure 1 The Statistics of the shipment of Global MEMS microphone market

This report focuses on how to solve the existing problems with prior art of charge pumps for MEMS driver applications, including the low driving efficiency issue as discussed before. To provide a fully integrated solution for the MEMS driver within a portable device, one of the biggest challenges is to generate a high voltage output efficiently (in order of 10V) from a low voltage input without breakdown. For these reasons, we need a high efficiency charge pump driver. In Chapter 2, a literature review of state of the art high voltage charge pump is introduced. Chapter 3 discusses the implementation details. Chapter 4 discusses the problems encountered during this Final Year Project. Chapter 5 outlines the conclusions and future works.

CHAPTER 2 LITERATURE REVIEW

2.1 Charge Pump Basics

There are several techniques can achieve the required high voltage output. Since this design is primarily intended for use on portable products, it is necessary to abandon the concept of using the high input voltage source. Therefore, adopting an extend of charge pump stage instead to achieve higher voltage output.

2.1.1 Dickson Charge Pump

In Chapter 1, the role and importance of MEMS in mobile devices has discussed. Allowing the MEMS to operate in a low phase noise environment [3], a high-level voltage supply should provide to the MEMS devices. Thus, a high-voltage charge pump is used to step up the low voltage input of the portable devices and emerge a high-level voltage pulse.

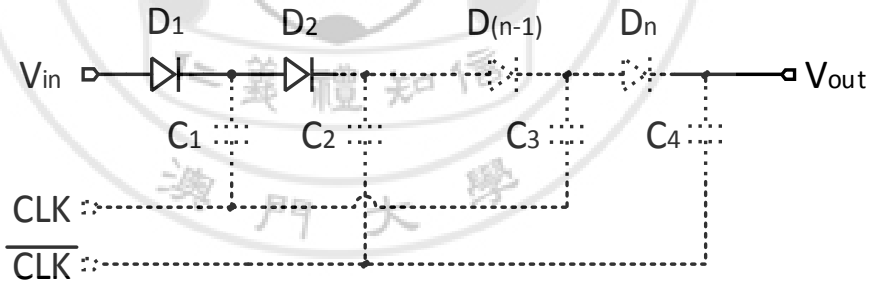

Figure 2 Schematic of Diode based Dickson Charge Pump

Fig. 2 shows an n-stage Dickson charge pump with diodes to produce a positive high output voltage Vout. By using two inverting clock phases, and in each stage, the capacitor will experience a charging and discharging process [4]. The charge pump doubles the output voltage of each stage, and increase the on-chip low voltage to the high voltage through the cascade. The fatal flaw in the Dickson Charge

Pump is that its power conversion is inefficient, which is mainly due to the loss of diode. In order to improve the power efficiency of charge pumps, most Dickson charge pumps use MOSFET instead of diodes. The main reason is that MOSFET's voltage loss is smaller than diodes. Considering that this design works primarily in a low-voltage environment, compared to PMOS, NMOS will be used to replace all the diodes in the Dickson Charge Pump. Mainly because the PMOS type Dickson Charge Pump cannot function properly under low voltage supply [5]. The modified Dickson Charge Pump is shown in Fig. 3.

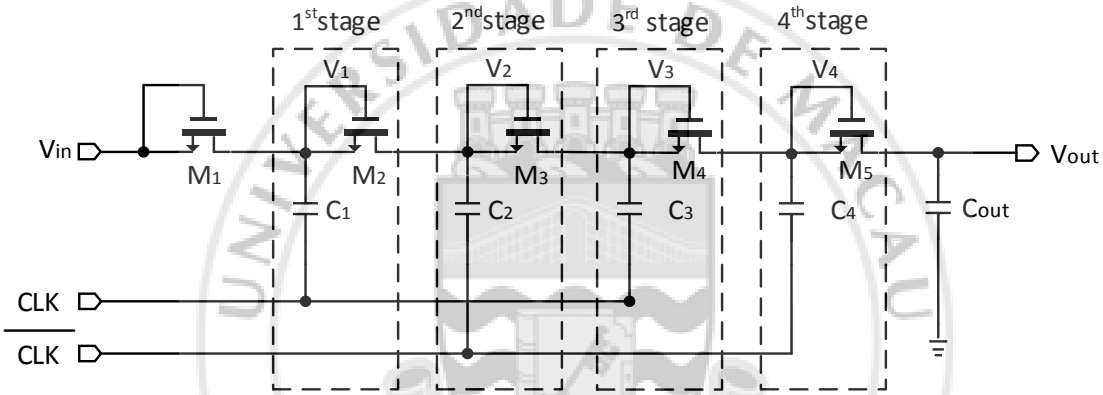

Figure 3 The modified Dickson Charge Pump by placing NMOS transistor instead of diode

The calculation shows below:

When CLK = 0;

$V_1 = V_{DD}$ and M_1 will turn off.

When CLK = V_{DD};

$V_1 = V_{DD} + V_{DD} = 2V_{DD}$

C_2 is charged by V_{IN} to $2V_{DD}$ via M_2, and V_2 will equal to $2V_{DD}$, M_2 will turn off.

$V_3 = 3V_{DD}$.

Therefore, $V_{OUT} = (N+1) \cdot V_{IN}$ Eq.1

Once consider with the Parasitic capacitance and the load, then the equation will become:

$$V_{OUT} = V_{IN} + N\left[\frac{C}{C+Cs} * V_{CLK} - V_{th} - \frac{I_{OUT}}{C+Cs} * f \right] - V_{th} \qquad \text{Eq.2}$$

$$\Delta V = [\frac{C}{C+Cs} * V_{CLK} - \frac{I_{out}}{C+Cs} * f \ ] \qquad \text{Eq.3}$$

$$G_V = \Delta V - V_{th} \qquad \text{Eq.4}$$

From the above equations 2 to 4, the output voltage of the charge pump is less than the theoretical value, which is affected by the following factors. The decrease of the ΔV and the presence of V_{th}. The voltage pump gain depends on the power supply voltage of the charge pump, and we can use cross-coupling techniques to solve this problem. Through the cross-coupled circuit technology, the dual pulse clock is used to charge and discharge the capacitor alternately. By controlling the connection between the PMOS and NMOS gates in the charge pump, the cross-coupled technology can reduce the reversion loss of the charge pump; therefore, the output voltage of this kind of charge pump can be more stable than the Dickson charge pump. Although the charge transfer switch provides a higher carrier speed, the threshold voltage drop through the switch will limit the output voltage level, resulting in the voltage pumping gain degradation.

2.2 State-of-the-art Charge Pump

The charge pump present in [1], is a high voltage driver in nanometer-scale. The two-level high voltage driver is implemented in 45-nm SOI CMOS technology, and the circuit implementation of the two-successive driver is shown below as Fig. 4.

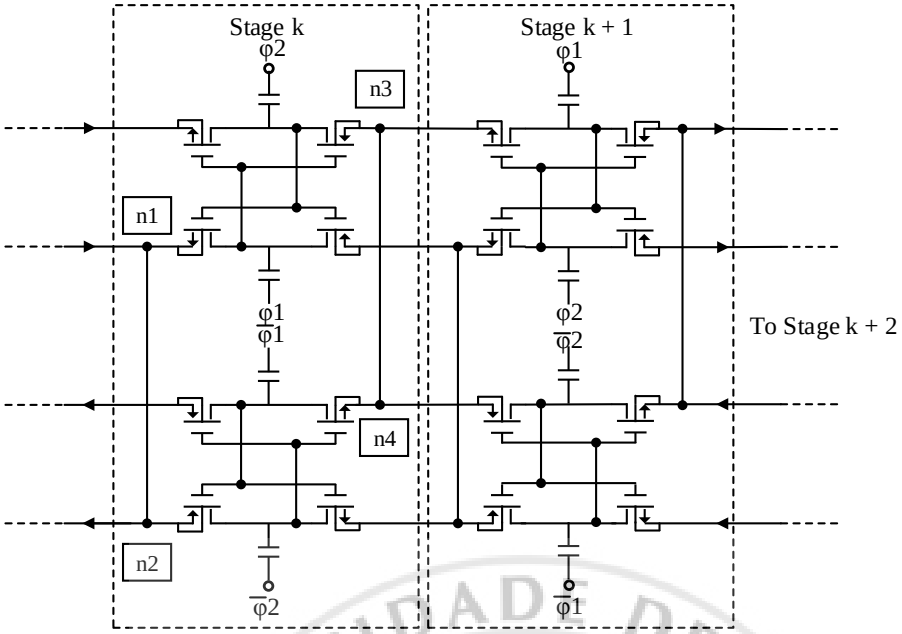

Figure 4 Proposed driver architecture of two successive driver stage in [1]

The above circuit uses a 45-nm SOI CMOS technology, rather than the bulk CMOS technology, for the following reasons: The first reason is that, for SOI CMOS technology, the breakdown limit of the buried oxide layer is significantly higher than in bulk CMOS. The second reason is that the SOI technology does not rely on reverse biased junctions for device isolation. As in the case with bulk CMOS technology, resulting in a higher speed at smaller power consumption for the design. From Fig. 3, we can see the node *n1* to *n4*. The nodes *n1* and *n3* connected to *n2* and *n4* respectively. This design ensures that the node voltage in the idle path is continuously followed by the node voltage of the active path, which can automatically refresh through the active-path capacitors.

Dual charge-transfer path design proposed in [1]. In addition to the benefit discussed in the previous paragraph, the design has its drawbacks. Now we presume that this design uses a specific frequency like f_{pump} and the drive resistance. The dual charge-transfer path is compared with the single path design, and the amount of energy consumed is twice as high. Because when a dual charge-transfer path design is

running, in each time the charging and discharging process. With the increase of total capacitance, power consumption will also increase relatively. This is one of the main reasons for the inefficiency of this design. In addition, in [1], the proposed architecture only uses two clock phase, if PMOS and NMOS switch connected at the same time, share the same gate drive, reversion loss will occur.

The calculation of Efficiency of a charge pump is:

$$\eta = \frac{E_{out}}{E_{in}} = \frac{E_{out}}{E_{out}+E_{loss}} \qquad \text{Eq.5}$$

For E_{in} is the energy supply by the V_{dd}, E_{loss} is the energy loss of the charge pump and E_{out} is the energy consumed by the load. Where E_{loss} consists of several types of losses such as conduction loss, redistribution loss, switching loss and reversion loss. All of these losses should be minimized to improve the efficiency of the charge pump [6]. Although the switches and capacitors are ideal, the redistribution loss will also be caused by two parallel capacitors. The "Break-before-make" mechanism is used to control the charge pump circuit, avoiding the overlap of the high clock phase, so that the reversion loss can be reduced and improves the efficiency of the design.

A modified charge pump output driver was introduced in [7]. Unlike [1], it decoupled the switch gate drive and adopted the "Break-Before-Make" mechanism mentioned in the previous paragraph. The circuit implementation of one-stage charge pump is shown below as Fig. 4.

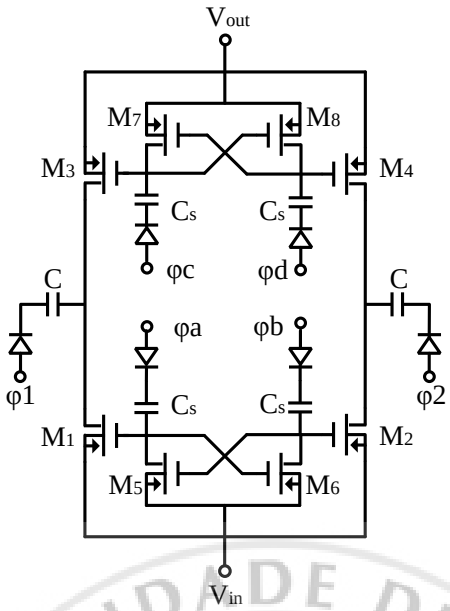

Figure 5 One stage of the proposed architecture in [7]

In the circuit of Fig.4, unlike [1], it gives up the design of a dual-charge transfer path instead of a single-charge transfer path. We can assume that compared to the dual-charge transfer path introduced in [1], it would be only about half the power loss. In general, for the state-of-the-art, their common problem is they make a direct connection between the output of the charge pump and the input of MEMS. The problem with this type of connection is that in each clock cycle, these designs will lose an amount of $\frac{1}{2}(C_L + C_p)$ of energy. It is impossible to avoid this loss for charge pump. But we can see that in this $\frac{1}{2}(C_L + C_p)$ energy loss, C_L is the load capacitance of the charge pump and C_p is the parasitic capacitor of MEMS. In this power loss, C_L accounts a large part (eg. $C_L > C_p$ by 10 times) of it. The C_L also has a certain impact on the rise / fall time limit. For instance, the $(C_L + C_p)$will charge up to $5V_{DD}$ and it will cause a longer rising/falling when compare with the capacitance C_p only. This project is going to solve these common problems of the recent art of charge pumps and will discuss in the following Chapter.

CHAPTER 3 IMPLEMENTATION DETAILS

3.1 System Overview

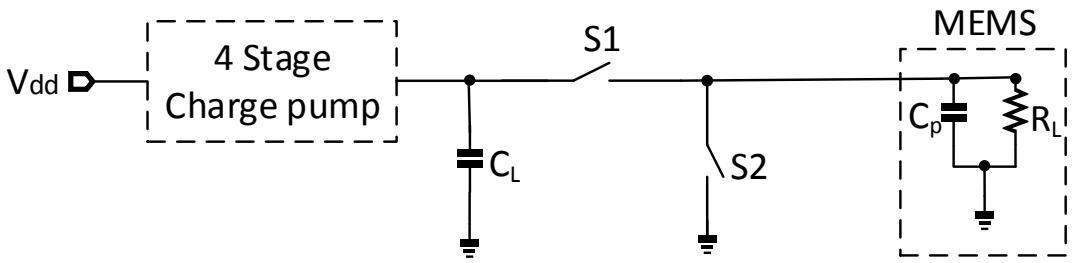

Figure 6 The block diagram of this work

The proposed architecture is shown in Fig. 6. To provide a fully integrated solution for the MEMS drivers within a portable electronic device. We apply a 4-stage charge pump to boost the low input voltage to the high voltage as required by MEMS. As discussed in Chapter 2, the most common problem of the state-of-the-art charge pumps is that they make a direct connection of the MEMS input with the charge pump output, resulting in a low system efficiency. For the purposed architecture, two switches are implemented to provide isolation between the loading capacitor of the charge pump and the parasitic capacitor of the MEMS. When the charge pump provides a voltage output of 4 times the V_{dd} by the two switches which mentioned before, this high voltage will transform to a high voltage square wave and pass to the MEMS input. To reduce the reversion loss, this design adopts the cross-coupling design and break-before-make mechanism introduced in Chapter 2. We will replace the 6-phase clock with a 4-phase clock, we will discuss that in the following paragraph. As shown in Fig. 6, because Vout is much larger than Vdd, if there is no switch to block them, there is a reversion loss that reduce the power conversion efficiency of the charge pump.

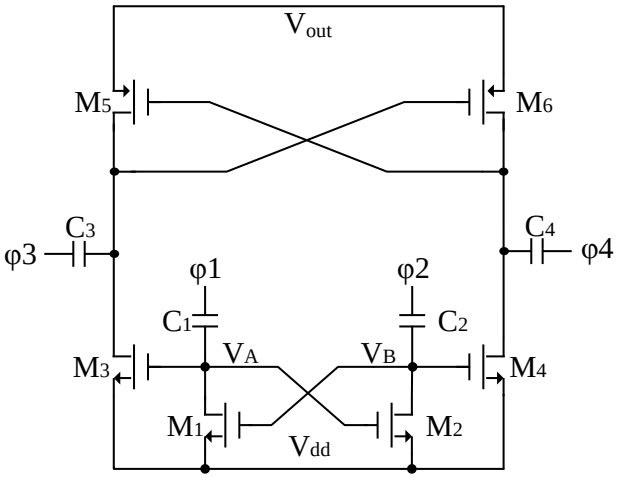

Figure 7 The proposed architecture of the charge pump

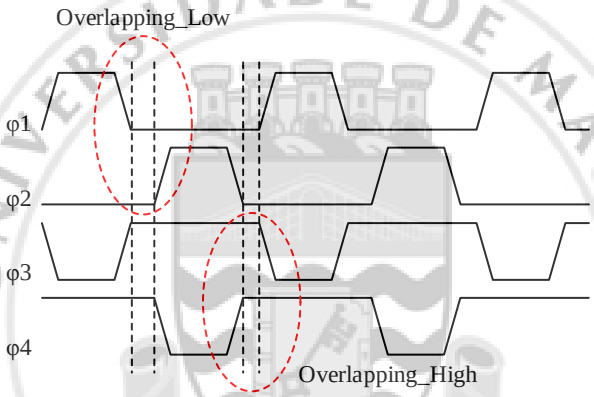

Figure 8 The non-overlapping clock phase working condition

Table 1 W/L ratio of the components of the charge pump

Transistor	Width(μm)	Length(nm)	W/L ratio
M1	1μ	240n	4.17
M2	1μ	240n	4.17
M3	1.6μ	240n	6.67
M4	1.6μ	240n	6.67
M5	3.6μ	240n	15.00
M6	3.6μ	240n	15.00

To avoid the connection between the high output voltage Vout with the low input voltage Vin, this work uses the break-before-make mechanism mentioned in the previous paragraph, which is a switch that is configured to break (open) the first set of connections before closing the new one. This prevents the momentary connection of the high and low voltage path. To fully understand the how it works, we refer to Fig.7 that shows the non-overlapping clock phases φ1 and φ2 and the inverse phases φ3 and φ4 respectively. As φ1 and φ2 are non-overlapping phases, there is a short duration such that φ1 and φ2 are low (Overlapping_Low), and the duration such that φ3and φ4 are high (Overlapping_high). The working condition of the proposed charge pump is that when φ1 =1, C_1 is charged to V_{dd} (Vin) and V_A = V_{dd}, thus turning M_2 off. With φ2 = 0, the lower plate of C_2 is charged up to V_{dd}, therefore the voltage at V_B is equal to 2 V_{dd} and turning on M_1 to fully charged the C_1. When φ2 = 1, the value of V_A and V_B are changed between V_{dd} and 2V_{dd}. Through M_3 and M_4, we can transfer the high charged voltage to the Vout, and adding the M_5 and M_6 which working with the break-before make mechanism, can helps to transfer the charged voltage (2Vdd) to the Vout.

For the proposed architecture of this work, as shown in Fig. 6, each capacitor is boosted directly through the clock phases, so the energy loss is less than the dual path charge design which apply in the recent charge pump, as shown in Fig. 3 in Chapter 2. This design differs from [7] in that it uses only four phase clocks instead of using six phase clocks for the following reasons. First, four phase clocks can also be implemented as break-before-make mechanism, so there is no need to use 6 phase clocks. The second reason is that the use of 6 phase clock will increase the difficulty in fine-tuning the non-overlapping time phases to achieve the break-before-make mechanism. Also, for the additional clock phase, we need to increase

the number of the level shifter relatively. So, the extra clock phases will increase the size of the entire design, resulting in increased cost. In this project, to achieve the design of unity, the four levels of charge pump will be implemented under the same circuit design concept, the design parameters of the charge pump are shown in table 1.

3.2 Detailed Implementation

Referring to Fig. 6, we assume that if the switch S1 does not exist in the work (the output of the charge pump and the MEMS is directly connected), the circuit must discharge both the C_L and C_P to generate a square wave to drive the MEMS. C_L is much larger that C_P, therefore the simultaneous discharge of C_L and C_P will result in a large amount of energy loss, mainly dominated by C_L. This is the main reason that the previous designs have the poor output power efficiency.

In order to improve the efficiency of this work, two sets of switches were set between charge pump and MEMS in this project. For the switch "S1" as shown in Fig. 6, it is used to disconnect the charge pump and the MEMS. It is also used to charge up the voltage of the MEMS 's C_p after it has discharged. The switch "S2" is mainly used to discharge the voltage of the MEMS's C_p and generate a square wave.

3.2.1 High Voltage Handling Switch

In this project, the integrated circuit mainly consists of CMOS transistors with a breakdown voltage of only 2.5V. Therefore, the problem encountered in this proposed architecture is mainly about how to modify the integrated circuit to handle the high output voltage which is 4X higher than the transistor breakdown voltage. In this Chapter, we first study the implementation of the conventional high voltage driver, and introduce the proposed solution in detail.

3.2.2 Conventional High Voltage Driver

The CMOS high voltage driver in [8] is composed of a p-switch block and a n-switch block, which are placed between the charge pump and the MEMS, and in parallel with the MEMS, respectively. Fig. 9 shows the n-switch block adopting the cascode topology. The stacked output transistors operate in the cut-off region or linear region altogether. The operation of the p-switch block is similar to the n-switch block but in complementary non-overlapping clock phases to prevent the short circuit current.

To understand the operation of the high voltage driver in [8], we can divide the n-switch block into two situations:

1. Driver output from low to high
2. Driver output from high to low.

In the first situation (i.e. the output changes from 0 to 3Vdd), the transistors M_1, M_2 and M_3 are initially in the linear region and nodes *n1*, *n2* are discharged. When the input port "In" changes from Vdd to 0, M_1 enters the cut-off region as $V_{GS} < V_{TH}$. Node *n1* is raised to V_{G2}, where V_{G2} is the gate voltage of M_2. Since the breakdown voltage of the transistor is Vdd, the gate of M_2 is connected to the bias voltage Vdd directly. Node *n2* is charged up to V_{G3}, the gate voltage of M_3. To prevent breakdown occurs, the gate of M_3 should connect to 2Vdd, which is generated by the resistive divider R_1 and R_2 between the output and the bias voltage Vdd through the transistor M_5. M_5 is in the linear region, and M_4 is in the cut-off region. As node *n2* is charged up to V_{G3}, M_3 enters the cut-off region. Here, the output voltage "out" is initially at 3Vdd.

In the second situation (i.e. the output changes from 3Vdd to 0), the transistors M_1, M_2 and M_3 are initially in the cut-off and nodes *n1*, *n2*, "out" are in different

voltage levels. When the input port "In" changes from 0 to Vdd, M_1 enters the linear region as $V_{GS} > V_{TH}$. The voltage of node *n1* is discharged to zero from V_{G2}. Consequently, the voltage of node *n2* is discharged to 0 from V_{G3}. To prevent breakdown occurs, now the gate of M_3 should connect to Vdd, which is generated by the bias voltage Vdd through the transistor M4, where M4 is controlled by the resistive divider R_3 and R_4. M_5 is in the cut-off region, and M_4 is in the linear region. As node *n2* is discharged to 0, M_3 enters the linear region. Here, the output voltage "out" is initially at 0.

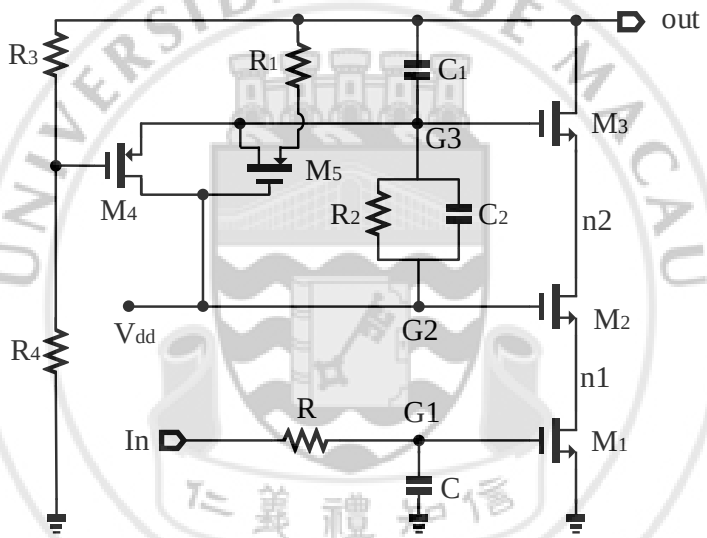

Figure 9 The schematic of the n-switch block from reference [8]

Fig. 10 summarizes the simulation results that demonstrate in the reference paper [8]. Fig. 10(a) shows that the voltage waveform of the output node "out" will generate a high voltage square wave at each cycle. Notice that the maximum voltage is less than 3Vdd. This voltage loss can reduce the system efficiency and must be considered in this project. By comparing the drain voltages (Fig. 10(a)) and gate voltages (Fig. 10 (b)), it is easier to understand the working principle of the high voltage driver. However, during the second situation, there is a risk of overshoot occur at the stacked transistors and this problem will be the discuss later in the Chapter 4.

The following Chapter is the proposed high voltage driver in the project. It is based on this conventional high voltage driver and make suitable adjustment to achieve the requirement of this project.

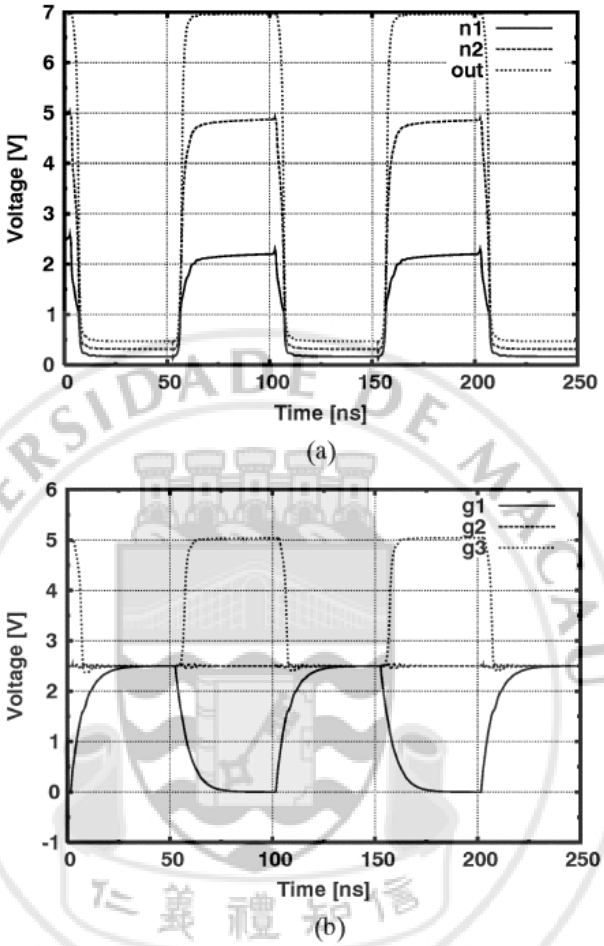

Figure 10 (a) Simulation results in [8] for the (a) drain voltages; and (b) gate voltages of M_1, M_2 and M_3.

3.2.3 Proposed High Voltage Driver

As discussed in the previous subchapter, the conventional high voltage driver in [8] cannot meet this project's requirement of 4Vdd output. This need to consider the voltage loss of the high voltage driver and the number of the stacked transistor of the switch blocks. And then modify the conventional high voltage driver in order to increase the output voltage to 4Vdd.

In this work, we propose a 4-stage charge pump with each stage cascaded on top of each other to achieve the requirement of 4Vdd output. As a result, each stage only handles 2.5 V. This voltage isolation ensures proper transistor operations without experiencing the breakdown issue, and is ultimately limited by the body diode breakdown.

Fig. 11 shows how the blocks replace the switches based on Fig. 6. Switch "S1" is replaced by the p-switch block and "S2" is replaced by the n-switch block. As mentioned before, the switch blocks are in complementary non-overlapping clock phases. Simply put, when p-switch is open, n-switch is closed and vice versa. By the mechanism of high voltage driver, it can replace the two switches between the charge pump output and MEMS input.

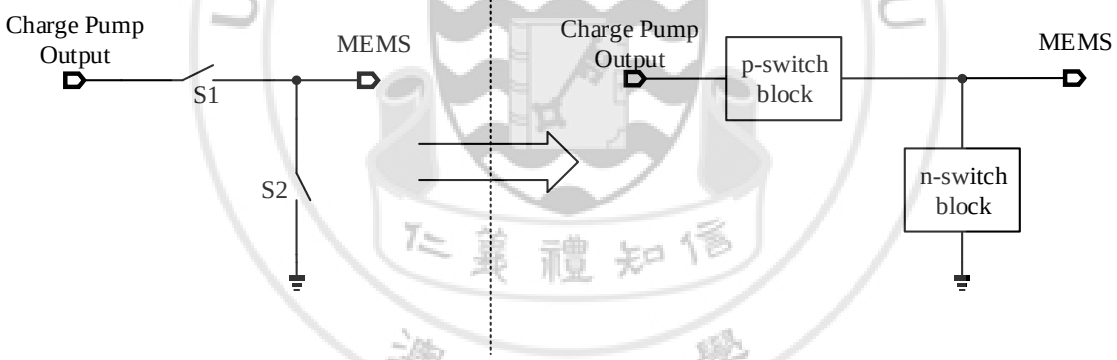

Figure 11 The relation between p/n-switch blocks and switches S1/S2

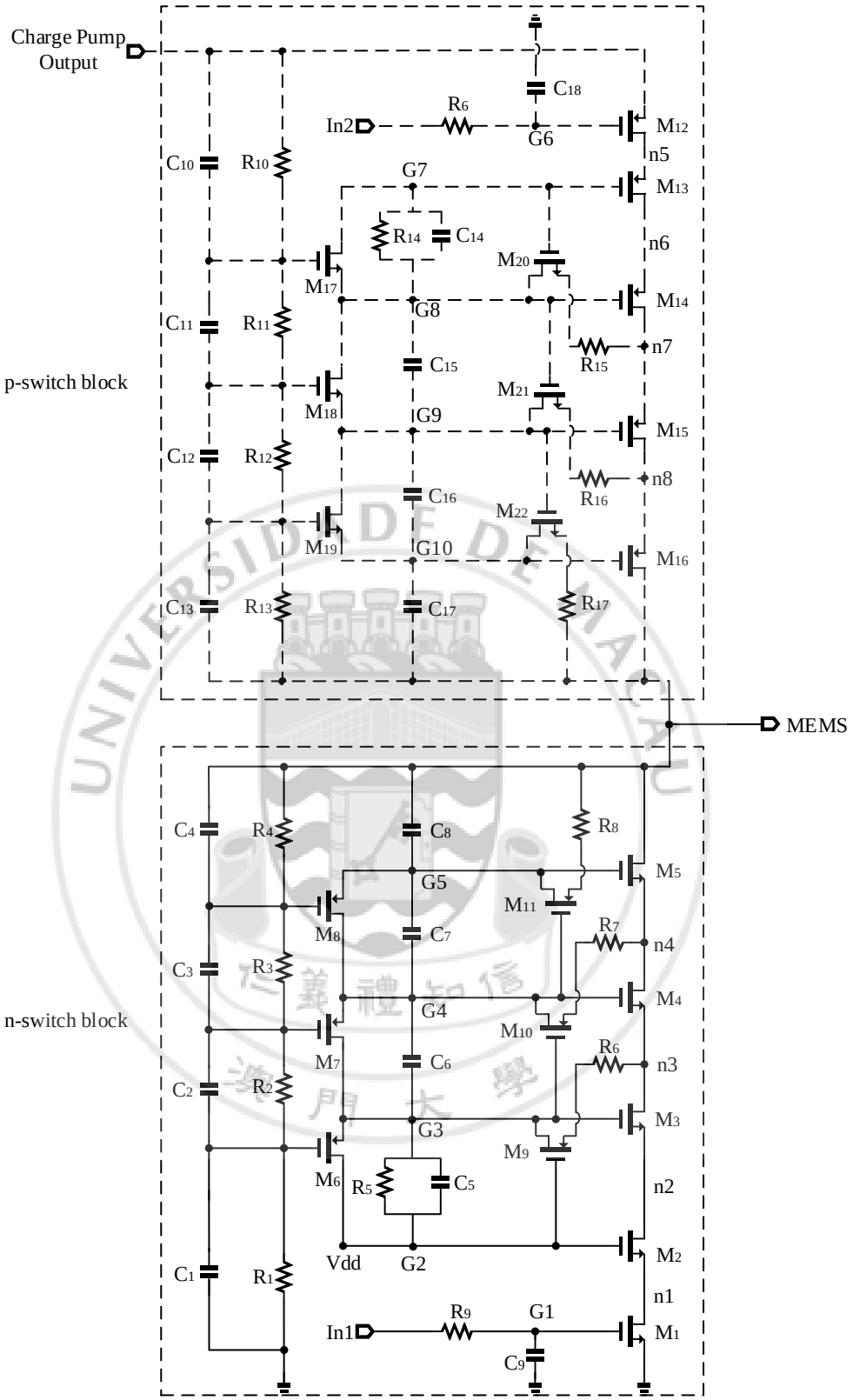

Figure 12 The schematic of the proposed high voltage driver

Table 2 W/L ratio of the components of the proposed high voltage driver

Transistor	Width(m)	Length(m)	W/L ratio
M_1	15µ	240n	62.5
M_2	60µ	240n	250
M_3	30µ	240n	125
M_4	50µ	240n	208.33
M_5	100µ	240n	416.67
M_6	320n	2µ	0.16
M_7	320n	2µ	0.16
M_8	320n	2µ	0.16
M_9	1µ	240n	4.17
M_{10}	1µ	240n	4.17
M_{11}	1µ	240n	4.17
M_{12}	40µ	240n	166.67
M_{13}	100µ	240n	416.67
M_{14}	50µ	240n	208.33
M_{15}	50µ	240n	208.33
M_{16}	150µ	240n	625
M_{17}	320n	2µ	0.16
M_{18}	320n	2µ	0.16
M_{19}	320n	2µ	0.16
M_{20}	320n	240n	1.33
M_{21}	320n	240n	1.33
M_{22}	320n	240n	1.33

Fig. 12 shows the detailed circuit implementation of the proposed high voltage driver and Table 2 shows the detailed sizes of the components. The upper part of Fig. 12 shows the p-switch block of the high voltage driver that used in this project, which represent the switch S1 in Fig. 11. The lower part shows the n-switch block which represent the switch S2 in Fig. 11. Each block has totally five stacks of transistors instead of four to achieve 4Vdd output. This is because the VDS drop of each stacked

transistor should be less than Vdd during practical operation. To ensure the output voltage can reach the voltage level of 4Vdd, the number transistors should be increased.

The design of this circuit is also expected to reduce the static power by enlarging the resistance of the resistors. These resistors are R_1, R_2, R_3, R_4 in the n-switch block and R_{10}, R_{11}, R_{12}, R_{13} in the p-switch block. Taking the n-switch block as an example, enlarge those resistors will increase the settling time of the gate voltage of M_6, M_7 and M_8. Consequently, this will make the gate voltage do not discharge to zero and cause breakdown in some of the transistors in the n-switch block. As the output is an AC signal, this problem can be solved by adding the capacitors C_1, C_2, C_3 and C_4 in parallel with the resistors to reduce the settling time.

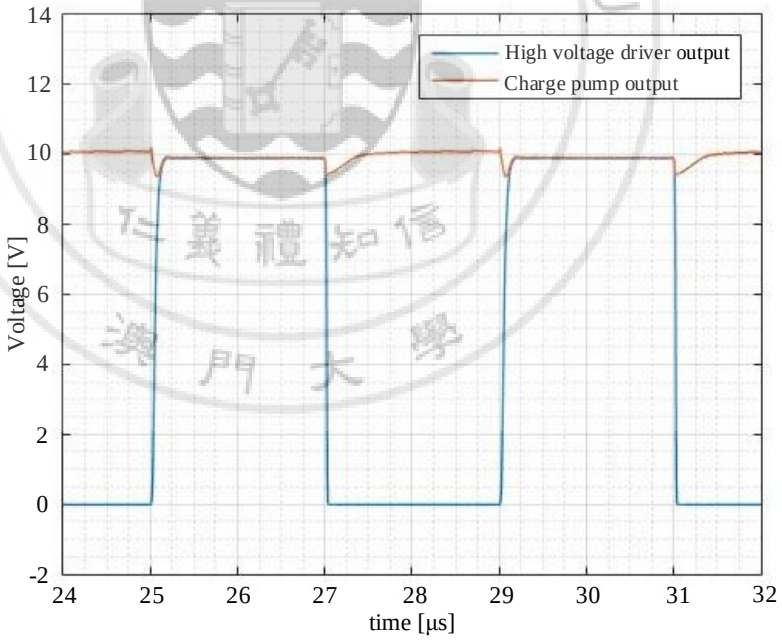

Figure 13 The outputs of the circuit

Fig. 13 shows the output waveforms of the high voltage driver and the charge pump. As shown in the graph, the charge pump output and driver output has the same voltage level 4Vdd (10V) in the time interval [25~27μs] and [29~31μs], otherwise the

voltage of the driver is 0. This combination gives a square wave to the input of the MEMS and satisfies the objective of the project.

To calculate the required transistor size (W/L ratio) to complete the switching operations, we define the driver efficiency equation as follows,

$$\eta = \frac{R_{load}}{R_{load}+R_{on}} \qquad \text{Eq.6}$$

$$\frac{W}{L} = \left(\frac{m}{KPR_{on}(V_{GS} - V_T)}\right)^{-1} \qquad \text{Eq.7}$$

where R_{load} represents the load resistance driven by the output driver, and R_{on} denotes the combined on-resistance of the stacked transistors, respectively. For the desired value of R_{on}, the W/L ratio of the stacked transistors can be found with the Eq.7, where m stands for the number of stacked transistors per switch block. In our project, m is 5 as we have five stacked transistors at each switch block, where KP, V_{GS}, V_T and (V_{GS} - V_T) is assumed to be fixed values. Therefore, to optimize the efficiency is mainly changing the W/L ratio of the transistors.

3.3 Layout Design

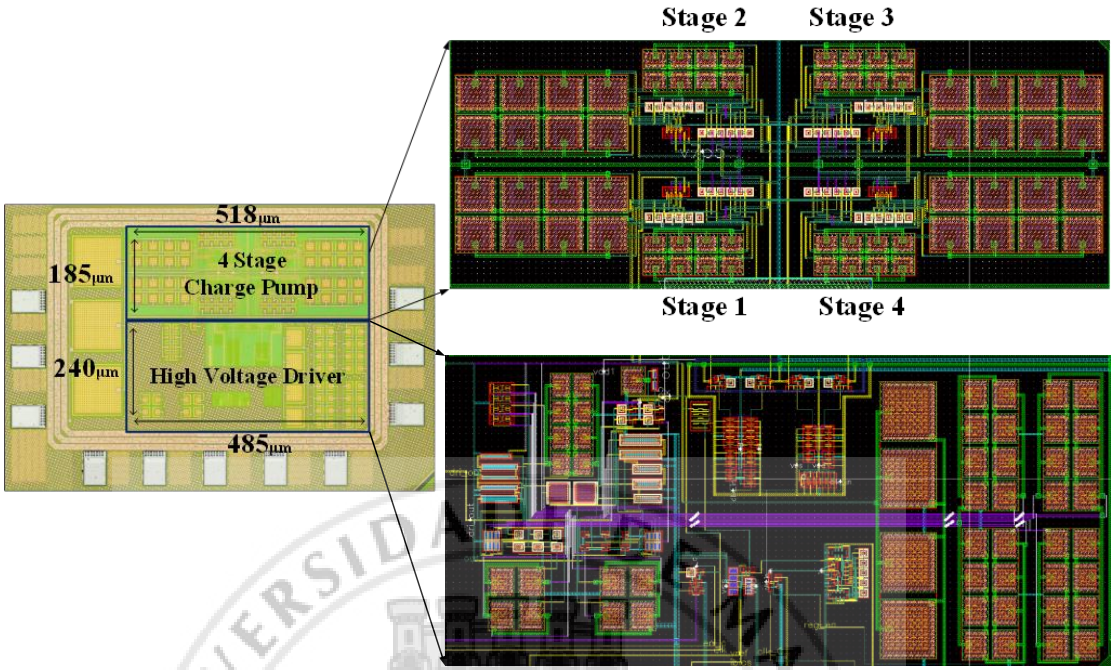

Figure 14 Micrograph of the 65nm CMOS die with all 4 sub-pumps and high voltage Driver high-lighted

The layout floorplan is for the upper part of the design, is the 4-stage charge pump and the lower part will be the high voltage driver and the regulation circuit. The Die micrograph with all four sub-pumps highlighted is shown in Fig. 14. The area of the 4 stage Charge pump and High Voltage Driver plus Regulation Circuit is 0.095mm^2 and 0.116mm^2 respectively. All the layout design is necessary clearances between high- and low- voltage metals. For instance, the metal spacing of the different type of component is critical. And there are some basic Design Rule should be aware, like the minimum width of the path of the different type of metal, for instance, if there is a large current passing through a narrow path, the path is considered like a fuse. Beside the minimum width of the path, the minimum spacing that mentioned before also need to be aware since we should avoid any unwanted short circuit between any polygon. After the basic design rules, there will be some advancing rules should be aware, they are: The Unit matching, the ideal situation is that two or more components

is equivalent component. Although the component A and B can be the same shape in area and perimeter, but they cannot be an identical item, as they are not with the same surrounding, therefore, the Dummies is adopted to have identical surrounding of the components.

Matching of the components of the layout, like transistor, resistor and capacitors etc. can effectively reduce random error, especially for the common centroid layout. It can reduce linear gradient error, and use the Guard Ring as a shield for isolation.

CHAPTER 4 Experimental Results

4.1 Voltage Overshoot

During the high to low driver output transitions, there is a risk of overshoot. This means that the transistor drain-source voltage drop V_{DS} of the stacked output transistors may be larger than its breakdown voltage Vdd. Fig. 15 illustrates how this problem can be resolved by employing the low-pass filter at the driver input.

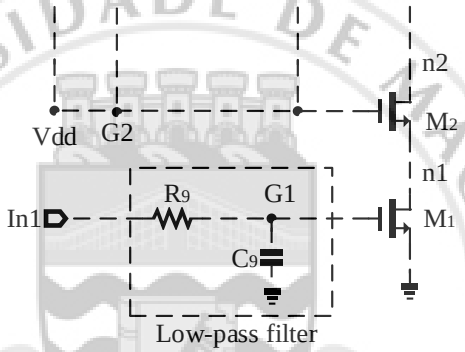

Figure 15 The low-pass filter (R_9, C_9) embedded at the gate of M1 of n-switch block

We first assume the case when the resistor R_9 and capacitor C_9 are removed. This means that "In1" is directly connected to the node g1 and gate of M_1, the input port "In1" is changed from low (0V) to high (Vdd) at the driver output high-to-low transition. The node g1 is connected to "In1", therefore M_1 enters the linear region and discharges the voltage at node n1. At node g2, there is a fixed biasing voltage Vdd at node g2 in the circuit, thus the voltage at node *n1* will affects the operating region of transistor M_2. Recall that Input port "In1" is a square wave input, the transistors M_1 and M_2 will have a delay in changing the cut-off region to linear region. In addition, voltage at n2 is slower than n1 to get discharge because M_2 is slower than M_1 to enter the linear region. Therefore, the voltage drop between the node *n2* and node *n1* (VDS of M2) may have an overshoot which larger than Vdd. To prevent this problem, the

low-pass filter that consists of resistor R_9 and capacitor C_9 is designed to delay the time of the node g1 to reach Vdd (2.5V), which is also mentioned in [8]. In the circuit, the values of R_9 and C_9 are 37.2008kΩ and 117.2832fF respectively. These values can satisfy the need of delay and prevent the overshoot happened at the stacked transistors. This low-pass filter will delay the rising edge to reach 2.5V and falling edge to reach 0V as shown in Fig. 16, thus the voltage of the V_{DS} and driver output will decrease. Modifications such as adjust the values between the W/L ratio of the transistors and the low-pass filter are needed to maintain the desired output. With other components in the circuit remain unchanged, Fig. 17 shows that there is overshoot under the condition of the low-pass filter disabled while Fig. 18 do not have overshoot under the condition of the low-pass filter enabled.

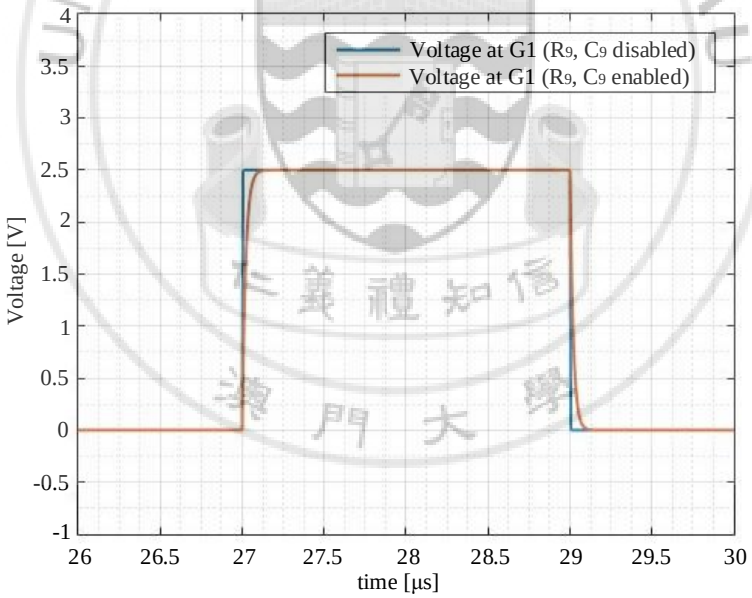

Figure 16 The voltage at node G1 under different condition

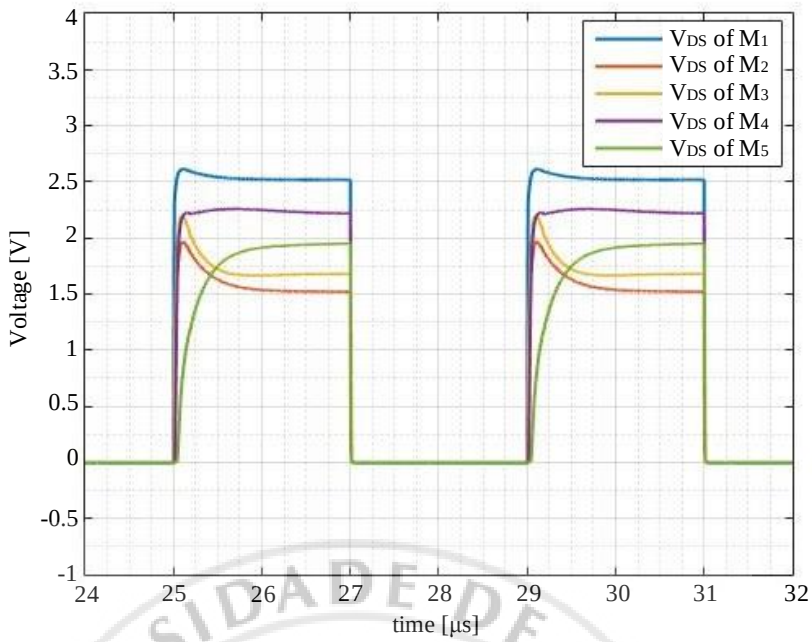

Figure 17 V_{DS} of stacked output transistors of the n-switch block without low-pass filter

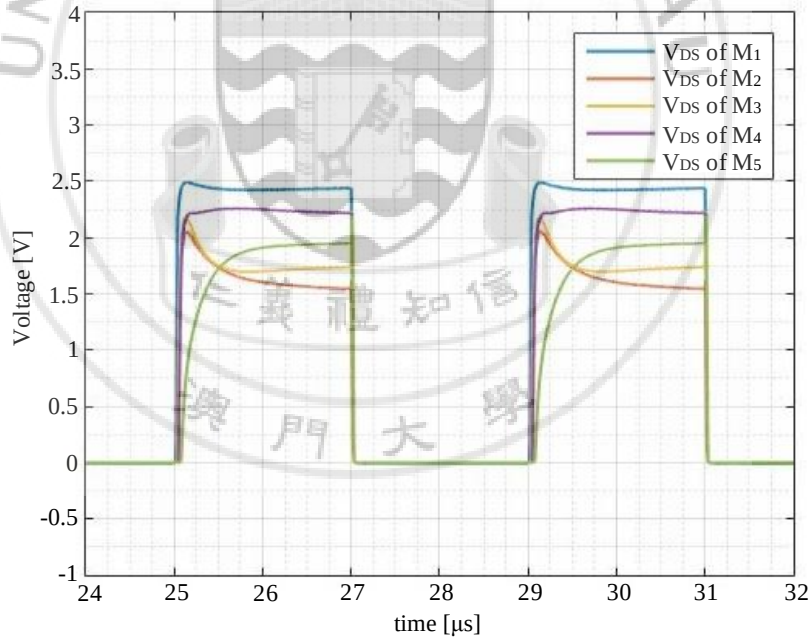

Figure 18 V_{DS} of stacked output transistors of the n-switch block with low-pass filter

4.2 Charge Sharing

When the switch between the two capacitors is closed and one of the capacitors is charging up by another one, the voltage level of the connection node will be degraded due to the charge redistribution mechanism. In the proposed architecture, the parasitic capacitance of the MEMS need to be charged and discharged to generate a square waveform. When it is connected back to the output of the charge pump, the output voltage of the charge pump will be degraded and less than 4Vdd instantly.

Fig.19 is the simulated output waveform of this project. In the graph, the two red and blue curves represent the voltage level of the charge pump output (voltage at load capacitor C_L) and the voltage level of the driver output (voltage at parasitic capacitor C_P of the MEMS), respectively. The vertical black dash-dotted line at the time 25μs represents the instance when the switch between the charge pump and MEMS is closed. On the left of the line, the switch between the charge pump and the MEMS is in open and the voltage of C_P is discharged to zero. On the other hand, the voltage of C_L is now kept the 4Vdd which comes from the output of charge pump. On the right of the line, the switch between the charge pump and MEMS is closed. The voltage at the output of the charge pump (voltage at C_L) starts to charge up the MEMS. From Fig.19, just after the time 25μs, the voltage of C_P starts to increase while the voltage of C_L starts to decrease to a certain voltage level. The voltage degradation occurs at C_L is caused by the charge sharing effect. Since the charge pump is in continuous operation, voltage of C_L will be charged back up to 4Vdd. On the other hand, the voltage of C_P will keep increasing and catch up the voltage of C_L after a certain time because the node is connecting now. These situations happen after the time 25μs as shown in Fig.19. In addition, the time needed for the capacitor to charge up is another problem

that it is impossible to generate a perfect square wave at the MEMS. This problem happened in the rising edge, therefore it is a bad influence on the operation speed and power efficiency.

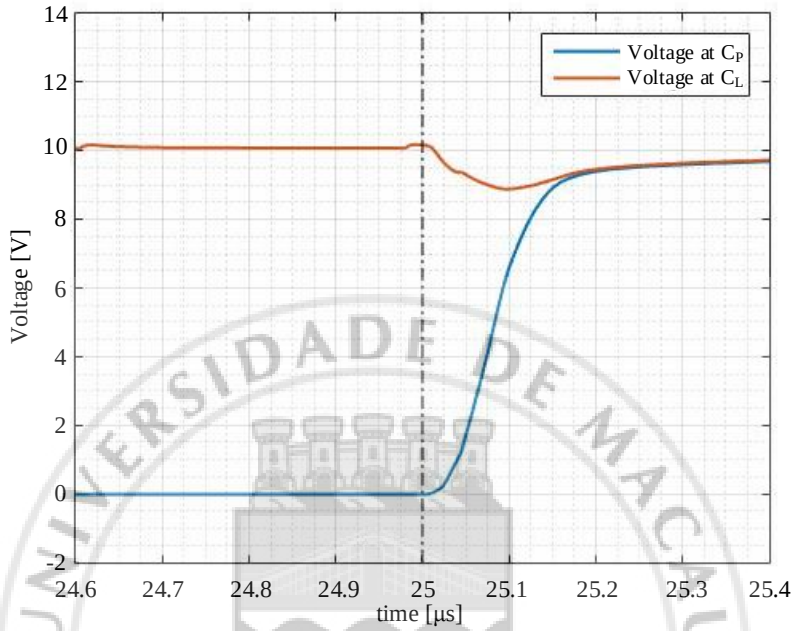

Figure 19 The illustration of the charge sharing

To improve the circuit performance, a charge sharing compensation capacitor Cc is added between the charge pump output and the input of the high voltage driver as shown in Fig. 20.

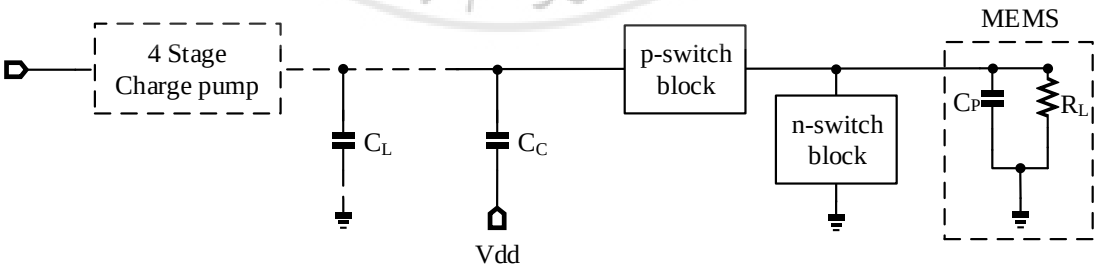

Figure 20 The schematic of the circuit with charge sharing compensation capacitor C_C

The top plate of the capacitor C_C has the same voltage level 4Vdd of C_L because they both connect to the charge pump output. The bottom plate of the capacitor C_C

will connect to a voltage supply. At the time when the charge pump starts to charge the MEMS, this voltage supply will provide extra charge to pump up the voltage at the top plate of the capacitor C_C immediately to compensate the charge sharing effects and shorten the rising time of the driver output. Fig. 21 shows the output waveform with the compensation capacitor C_C. The rising time of the voltage at C_P is much shorter than the one that show in Fig. 19. Fig. 22 shows the output waveform of voltage under the appearance of C_C. The red curve is the voltage at C_P with C_C enabled while the blue curve is the voltage at C_P with C_C disabled. Obviously, when C_C is enabled, the rising time of the edge is much shorter. The rising time of the red curve is 80ns, while the rising time of the blue curve is about 120ns. The rising time with C_C enabled is 40ns faster to rise back to high potential. In addition, the voltage degradation of the charge pump output has been reduced, which means that it is quicker to charge back to 4Vdd (10V).

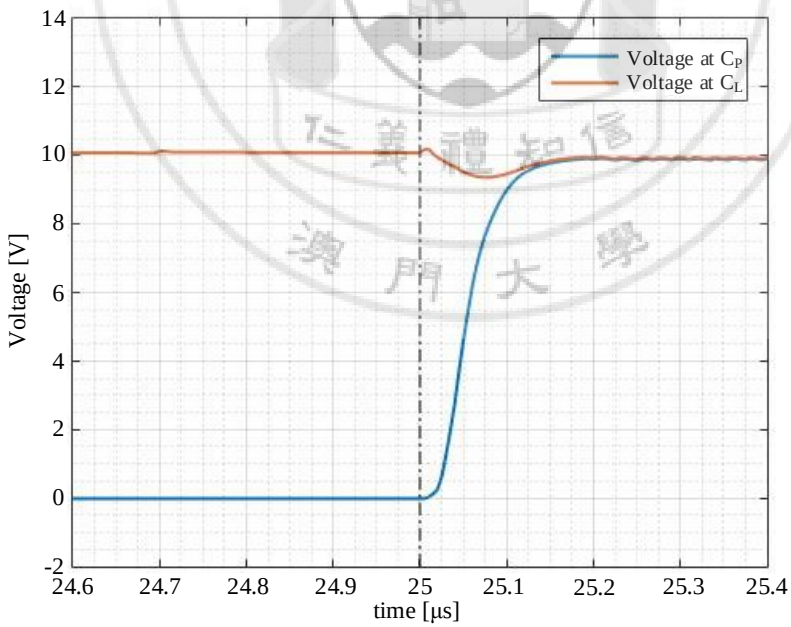

Figure 21 The outputs with compensation capacitor C_C

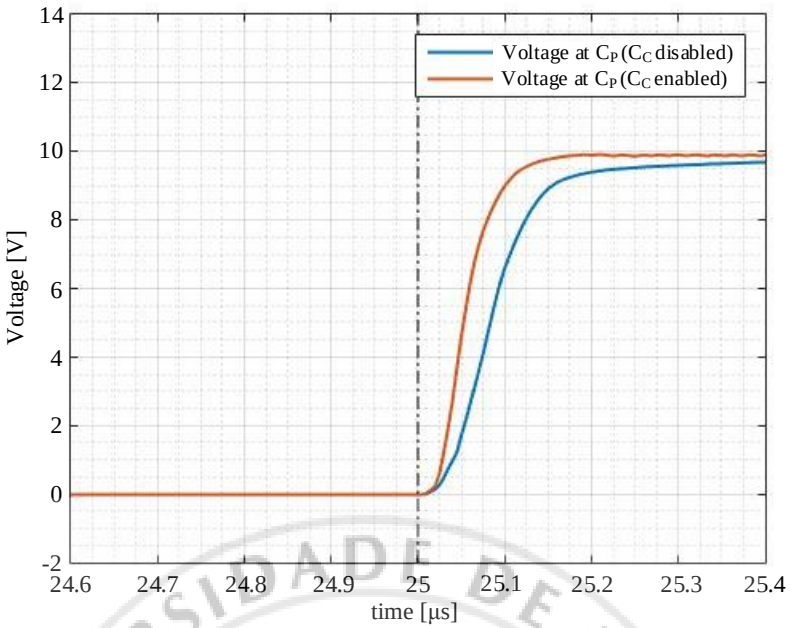

Figure 22 The driver outputs under the appearance of C_C

4.3 Chip Measurement Results

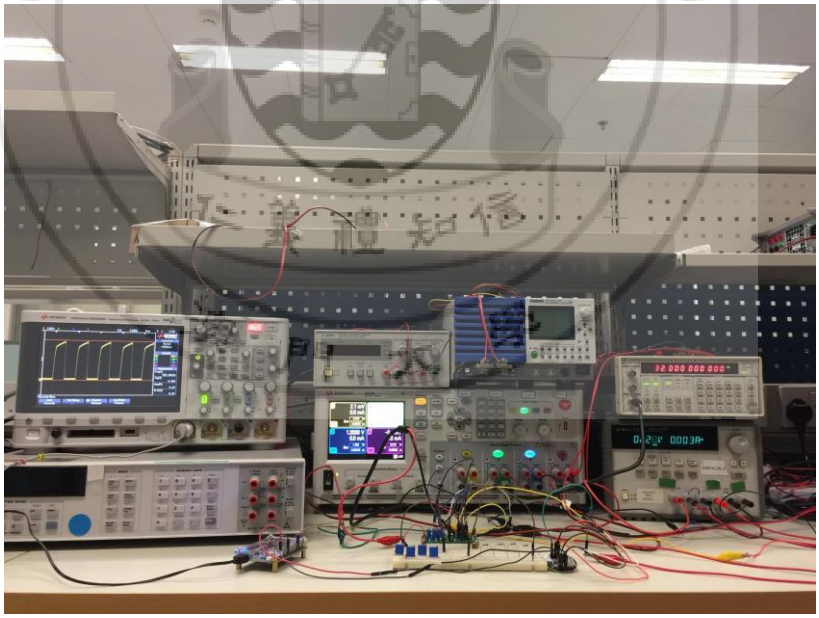

Figure 23 Measurement setup of the chip prototype

Fig. 23 shows the measurement setup of the chip prototype. It is composed of a digital power supply, an external clock source, a digital multimeter for accurate voltage/current measurement, an oscilloscope to observe the output waveform, and an FPGA for control generation.

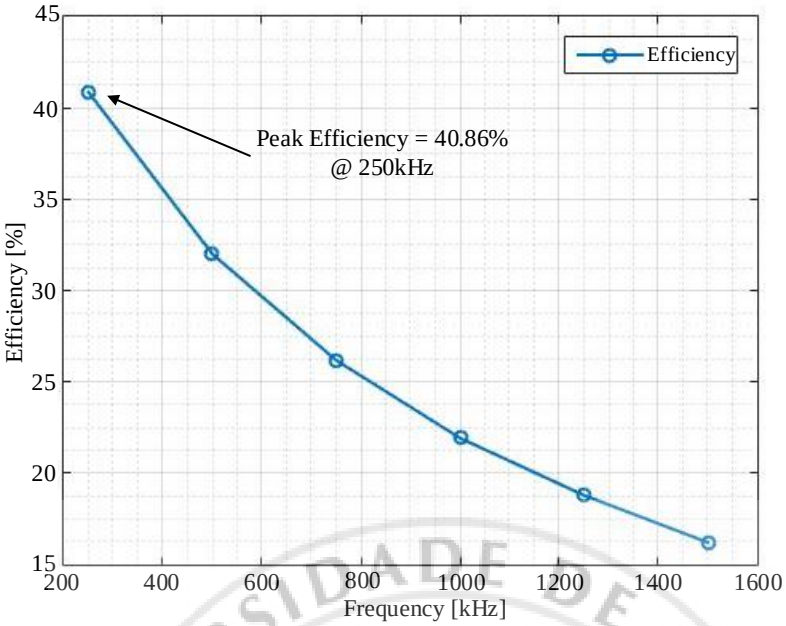

Figure 24 The efficiency of the MEMS Drivers

The simulation result of the MEMS Drivers is shown in Fig.24. The input frequency varies from 250kHz to 1500kHz, with load current and load capacitance of 100μA and 5pF, respectively. From Fig.24, it is easy to discover that the efficiency is inversely proportional to the input frequency. At 250kHz, its peak efficiency is about 40.86%, and while in 1500kHz the efficiency drop to 16.21%. If the input frequency is higher than 1500kHz, the voltage level of the driver output starts to decline and cannot reach to 4Vdd. We can understand that the frequency of the switch is too fast, causing the incapability of the driver to charge up to 4Vdd before discharge. Therefore, the input frequency that higher than 1500kHz will not be considered.

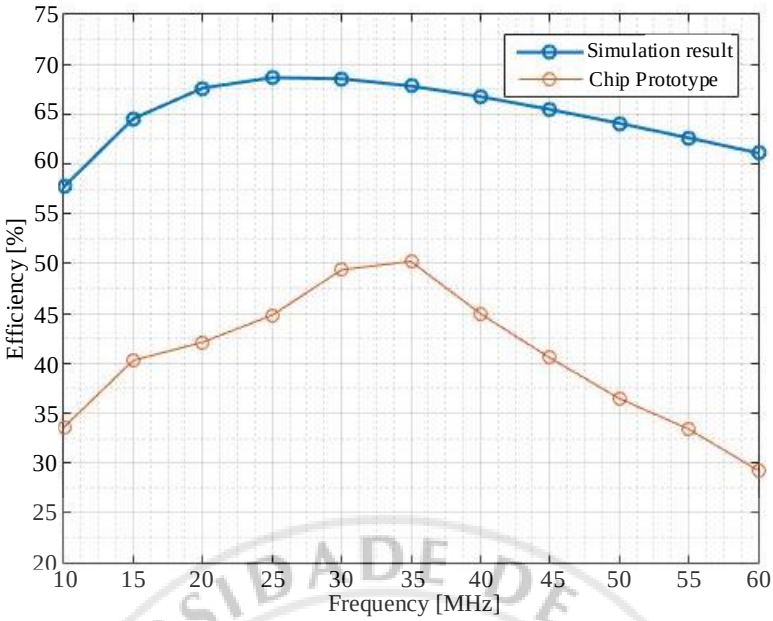

Figure 25 The comparison of the simulation and chip measurement results

The simulation result of the charge pump efficiency and the measurement of the chip prototype is shown in Fig.25. The input frequency is between 10MHz to 60MHz, and the load resistance is 100kΩ. From the above figure, the efficiency of the simulation and the PCB result varies between 55% to 70% and 30% to 50%, respectively. This means that the efficiency difference between the simulation results and the chip measurement results is about 20%.

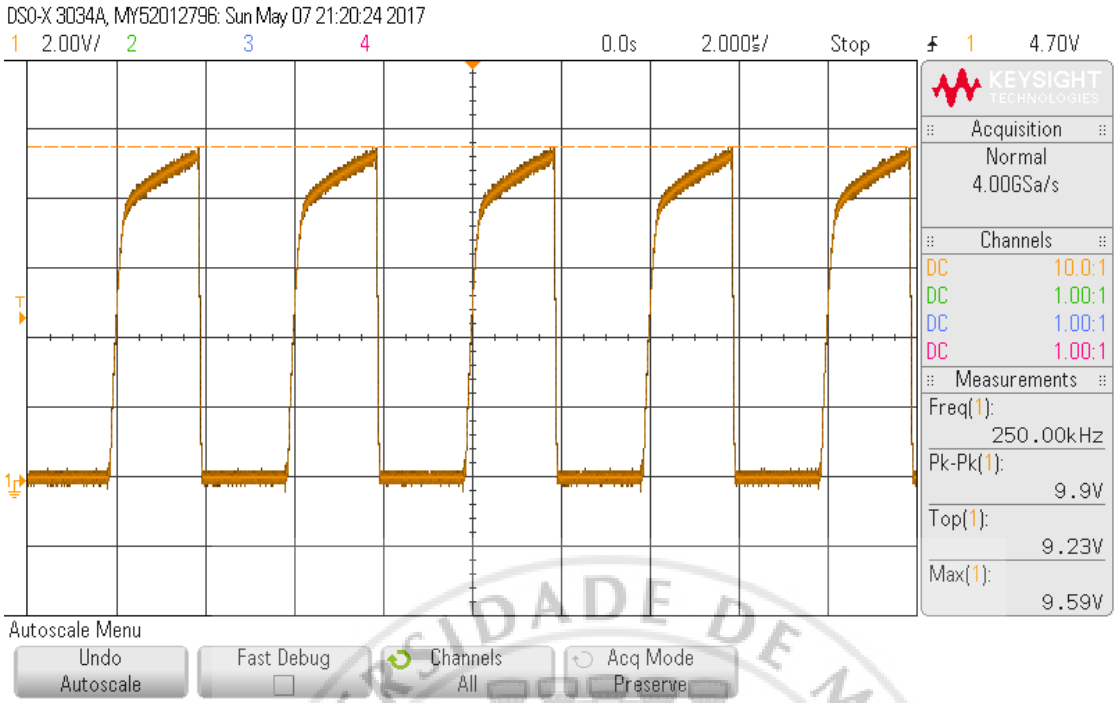

Figure 26 Measurement result of chip prototype

The measurement result of the chip prototype is shown in Fig. 26. The input frequency of the charge pump and high-voltage drivers is 32MHz and 250kHz, respectively. the chip prototype can successfully provide the square wave output with peak to peak voltage 9.9V as shown in Fig. 26. Although the peak to peak voltage is 9.9V, the high stage of the square wave is not as like as the flat output waveform that shown in Figure 13. Furthermore, the efficiency of the chip prototype differs from the efficiency that which shown in Fig. 24, which means that the chip result has a poor efficiency when compare with the simulation result.

Here are the errors that may occur during the chip measurement. For instance, the input current that supply form the machine to the PCB is different from the simulation, the passive probe of the oscilloscope is only 10MΩ and has a capacitive load with 4pF. Therefore, there is a loading effect occur during the experiment, etc.

CHAPTER 5 Summary of this work

5.1 Comparison with recent works5.1 Comparison with recent works

Table 3 Summary of the recently work

	ASSCC2014 [7]	ISSCC2014 [3]	JSSC16 [2]	**This work**
Technology(nm)	65	65	130	**65**
Number of Stage	5	17	3	**4**
Voltage Range	12	34	10	**10**
Square Wave Output	Yes	No	Yes	**Yes**
Peak Charge Pump Efficiency	63.5%*	38%*	77%*	**68.6%#** **50.2%***
Driver efficiency (@ 250kHz)	4.7%◎	--	4.35%◎	**40.86%#**
Rise/fall time(ns)	330/330	--	513/513	**80/35**

* Measurement result of chip prototype
\# Simulation result
◎ Extracted from the paper

From table 3, two of the three charge pump efficiency is inversely proportional to the number of stage of the charge pump. Since the more of the stage of charge pump, the more of the power loss. In addition, the driver efficiency of the previous work is low and unsatisfied, one of the main reason is that there is a huge power loss of the discharging process mentioned in the previous parts.

5.2 Conclusion

This report discussed the design of Dickson's charge pump and the state of the art techniques for charge pump design. During this process, we discovered that the common problems are the rise/fall time limits, and the low driver efficiency of ~4%. To address these problems, this report has adopted the advanced high-voltage driver which discussed in [8], to reduce the energy loss in the charge pump's load capacitor, since the capacitance of C_L is much larger than the parasitic capacitance C_p of the MEMS. If C_L discharges in each clock cycle, a large power loss will cause since the loss of power depends on the value of C_L. This work has attempted to improve the power efficiency of the circuit by resolving the power loss caused by C_L.

This report included the design of a fully-integrated high-voltage MEMS driver implemented in a 2.5-V 65-nm CMOS technology. The driver includes a charge pump, a high-voltage driver and a charge-sharing compensation capacitor, etc. Comparing with the output efficiency of the state-of-the-art drivers, this project shows a more favorable peak efficiency of 40.86% at an input frequency of 250kHz.

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